Appellants further challenge the motivation for taking bandpass filter-amplifier means 74 of Hughes and sticking it in a phase lock loop modified by Sutardja in view of Nardi as suggested by the Examiner.

Appellants further submit that Sutardja teaches power supply rejection capabilities to reduce phase noise and jitter as previously described above. Yet, Hughes teaches directly receiving signals from a power line which is an extremely noisy power supply. Respectfully, Hughes and Sutardja teach away from each other and should not be combined.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 7.

VIII. Group VIII: Claim 14

Claim 14 stands rejected as being obvious over Sutardja in view of Nardi, and further in view of Hughes. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section VIII with respect to claim 14.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on the combination of Sutardja and Nardi with respect to claim 14.

In addition, claim 14 recites "a limiter coupled between the bandpass filter and the first input of the phase detector". Since at least these elements of claim 14 are the same as the elements recited above with respect to claim 11, the arguments made in Section V with respect to claim 11 are made here in Section VIII with respect to claim 14. In addition, Hughes does not make up for the teaching deficiencies of Sutardja in view of Nardi. Hughes is silent as a limiter to limit a filtered mixed signal before being applied to a phase detector.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the

obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 14.

Furthermore, Appellants respectfully submit that Hughes teaches away from the alleged motivation for combining Sutardja, Nardi and Hughes which, according to the Examiner, "to employ a phase modulator in conjunction with a resonator in order to realize a phase locking oscillator circuit having a loop bandwidth broader than that of existing oscillator circuits". Office Action Made Final of April 22, 2005 at page 12. Nardi at FIG. 2 shows that the reason for expanding the loop bandwidth is because as phase noise of the reference oscillator 18 improves, to take advantage of the favorable phase noise plot as illustrated in FIG. 2, the loop bandwidth needs to be expanded beyond at least 10^6 radians. Compare this with Hughes, which is a power line communications system that operates at 60 Hz. To incorporate bandpass filter-amplifier means 74 of Hughes would effectively decrease loop bandwidth if the bandpass filter-amplifier means 74 were inserted into the Sutardja circuit modified by the Nardi circuit.

Appellants respectfully submit that one of ordinary skill in the art would not look to Hughes which operates at a system-wide frequency of 60 Hz for teachings to expand loop bandwidth beyond at least 10^6 radians. Furthermore, since the bandpass filter-amplifier means 74 is not part of phase lock loop 64 found in Hughes at FIG. 1D, Appellants further challenge the motivation for taking bandpass filter-amplifier means 74 of Hughes and sticking it in a phase lock loop modified by Sutardja in view of Nardi as suggested by the Examiner.

Appellants further submit that Sutardja teaches power supply rejection capabilities to reduce phase noise and jitter as previously described above. Yet, Hughes teaches directly receiving signals from a power line which is an extremely noisy power supply. Respectfully, Hughes and Sutardja teach away from each other and should not be combined.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 14.

IX. Group IX: Claim 21

Claim 21 stands rejected as being obvious over Sutardja in view of Nardi, and further in view of Hughes. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section IX with respect to claim 21.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on the combination of Sutardja and Nardi with respect to claim 21.

In addition, claim 21 recites "means for limiting the filtered mixed signal from the filter means before being applied to the detector means". Since at least these elements of claim 21 are the same as the elements recited above with respect to claim 18, the arguments made in Section VI with respect to claim 18 are made here in Section IX with respect to claim 21.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 21.

Furthermore, Appellants respectfully submit that Hughes teaches away from the alleged motivation for combining Sutardja, Nardi and Hughes which, according to the Examiner, "to employ a phase modulator in conjunction with a resonator in order to realize a phase locking oscillator circuit having a loop bandwidth broader than that of existing oscillator circuits". Office Action Made Final of April 22, 2005 at page 12. Nardi at FIG. 2 shows that the reason for expanding the loop bandwidth is because as phase noise of the reference oscillator 18 improves, to take advantage of the favorable phase noise plot as illustrated in FIG. 2, the loop bandwidth needs to be expanded beyond at least 10^6 radians. Compare this with Hughes, which is a power line communications system that operates at 60 Hz. As alleged by the Examiner, to incorporate bandpass filter-amplifier means 74 of Hughes would effectively decrease loop bandwidth if the bandpass filter-amplifier means 74 were inserted into the Sutardja circuit modified by the Nardi circuit.

Appellants respectfully submit that one of ordinary skill in the art would not look to Hughes which operates at a system-wide frequency of 60 Hz for teachings to expand loop bandwidth beyond at least 10^6 radians. Furthermore, since the bandpass filter-amplifier means 74 (which the Examiner alleges is filter means with respect to claim 21) is not part of phase lock loop 64 found in Hughes at FIG. 1D, Appellants further challenge the motivation for taking bandpass filter-amplifier means 74 of Hughes and sticking it in a phase lock loop modified by Sutardja in view of Nardi as suggested by the Examiner.

Appellants further submit that Sutardja teaches power supply rejection capabilities to reduce phase noise and jitter as previously described above. Yet, Hughes teaches directly receiving signals from a power line which is an extremely noisy power supply. Respectfully, Hughes and Sutardja teach away from each other and should not be combined.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 21.

X. Conclusion

For the foregoing reasons, claims 1-21 are patentable over the alleged prior art of record. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: October 25, 2005

Respectfully submitted,

Michael T. Cruz

Michael T. Cruz
Registration No. 44,636

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
Telephone: (312) 775-8084
Facsimile: (312) 775-8100

APPENDIX

The following claims are involved in this appeal:

1. A complimentary metal oxide semiconductor (CMOS) phase lock loop, comprising:

an oscillator having a tuning input, and an output with a tunable frequency responsive to the tuning input;

a mixer to mix the oscillator output with a second signal to produce a mixed signal; and

a phase detector outputting an error signal which is a function of a phase difference between the mixed signal and an input signal, the error signal being applied to the tuning input.

2. The CMOS phase lock loop of claim 1 wherein the oscillator comprises a voltage controlled oscillator, the tuning input being responsive to a voltage of the error signal.

3. The CMOS phase lock loop of claim 1 further comprising a bandpass filter to filter the mixed signal before being applied to the phase detector, the filtered mixed signal comprising a difference frequency between the tuned frequency of the oscillator output and a frequency of the second signal.

4. The CMOS phase lock loop of claim 3 further comprising a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector.

5. The CMOS phase lock loop of claim 1 further comprising a charge pump disposed between the phase detector and the oscillator.

6. The CMOS phase lock loop of claim 1 further comprising a loop filter disposed between the phase detector and the oscillator.

7. The CMOS phase lock loop of claim 1 wherein the oscillator comprises a voltage controlled oscillator, the tuning input being responsive to a voltage of the error signal, the CMOS phase lock loop further comprising a bandpass filter to filter the mixed signal before being applied to the phase detector, the filtered mixed signal comprising a difference frequency between the tuned frequency of the oscillator output and a frequency of the second signal, a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector, a charge pump disposed between the phase detector and the oscillator, and a loop filter disposed between the charge pump and the oscillator.

8. A complimentary metal oxide semiconductor (CMOS) phase lock loop, comprising:

a tunable oscillator having a tuning input;

a mixer coupled the oscillator; and

a phase detector having a first input coupled to the mixer, a second input adapted to receive an input signal, and an output coupled to the tuning input.

9. The CMOS phase lock loop of claim 8 wherein the oscillator comprises a voltage controlled oscillator.

10. The CMOS phase lock loop of claim 8 further comprising a bandpass filter coupled between the mixer and the first input of the phase detector.

11. The CMOS phase lock loop of claim 10 further comprising a limiter coupled between the bandpass filter and the first input of the phase detector.

12. The CMOS phase lock loop of claim 8 further comprising a charge pump coupled between the phase detector output and the tuning input of the oscillator.

13. The CMOS phase lock loop of claim 8 further comprising a loop filter coupled between the phase detector output and the tuning input of the oscillator.

14. The CMOS phase lock loop of claim 8 wherein the oscillator comprises a voltage controlled oscillator, the CMOS phase lock loop further comprising a bandpass filter coupled to the mixer, a limiter coupled between the bandpass filter and the first input of the phase detector, a charge pump coupled to the phase detector output, and a loop filter coupled between the charge pump and the tuning input of the oscillator.

15. A complimentary metal oxide semiconductor (CMOS) phase lock loop, comprising:

oscillator means for generating a first signal having a tunable frequency, the oscillating means comprising tuning means for tuning the frequency of the first signal;

mixer means for mixing the first signal with a second signal to produce a mixed signal; and

detector means for detecting a phase difference between the mixed signal and an input signal, and generating an error signal which is a function of the phase difference, the tuning means being responsive to the error signal.

16. The CMOS phase lock loop of claim 15 wherein the oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal.

17. The CMOS phase lock loop of claim 15 further comprising filter means for filtering the mixed signal before being applied to the detector means, the filtered mixed signal comprising a difference frequency between the tuned frequency of the first signal and a frequency of the second signal.

18. The CMOS phase lock loop of claim 17 further comprising means for limiting the filtered mixed signal from the filter means before being applied to the detector means.

19. The CMOS phase lock loop of claim 15 further comprising means for sourcing current to the tuning means responsive to the error signal.

20. The CMOS phase lock loop of claim 15 further comprising means for filtering the error signal from the detecting means before being applied to the tuning means.

21. The CMOS phase lock loop of claim 15 wherein the oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal, the CMOS phase lock loop further comprising filter means for filtering the mixed signal before being applied to the detector means, the filtered mixed signal comprising a difference frequency between the tuned frequency of the first signal and a frequency of the second signal, means for limiting the filtered mixed signal from the filter means before being applied to the detector means, current means for sourcing current to the tuning means responsive to the error signal, and means for filtering the current sourced error signal from the current means before being applied to the tuning means.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. 15258US08

In the Application of:

Ahmadreza Rofougaran et al.

U.S. Serial No.: 09/698,498

Filed: October 27, 2000

For: ADAPTIVE RADIO TRANSCEIVER WITH NOISE SUPPRESSION

Examiner: Marceau Milord

Group Art Unit: 2682

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I hereby certify that this correspondence is being sent via facsimile transmission to the United States Patent and Trademark Office at (571) 273-8300 on October 25, 2005.

Michael T. Cruz
Michael T. Cruz
Reg. No. 44,636

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Notice of Appeal was received by the United States Patent and Trademark Office on July 25, 2005 for the above-identified patent application. A Petition for a One-Month Extension has been enclosed, thereby extending the deadline for filing an Appeal Brief in support of the Notice of Appeal to October 25, 2005.

REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 16215 Alton Parkway, Irvine, California 92618-3616, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment filed with the present application and recorded on Reel 011785, Frame 0092.

RELATED APPEALS AND INTERFERENCES

There are currently no appeals pending regarding related applications.

STATUS OF THE CLAIMS

Claims 1-21 are pending in the present application. Pending claims 1-21 have been rejected under 35 U.S.C. § 103(a) and are the subject of this appeal.

STATUS OF THE AMENDMENTS

There are no amendments pending in the present application.

SUMMARY OF THE INVENTION

Some embodiments according to some aspects of the present invention may provide, for example, a complimentary metal oxide semiconductor (CMOS) phase lock loop that may include, for example, an oscillator, a mixer and a phase detector. The oscillator may have, for example, a tuning input and an output with a tunable frequency responsive to the tuning input. The mixer may mix, for example, the oscillator output with a second signal to produce a mixed signal. The phase detector may output, for example, an error signal which is a function of a phase difference between the mixed signal and an input signal. The error signal may be applied, for example, to the tuning input.

Some embodiment according to some aspects of the present invention may provide, for example, a CMOS phase lock loop that may include, for example, a tunable

oscillator, a mixer and a phase detector. The tunable oscillator may have, for example, a tuning input. The mixer may be coupled, for example, to the oscillator. The phase detector may have, for example, a first input coupled to the mixer, a second input adapted to receive an input signal, and an output coupled to the tuning input.

Some embodiments according to some aspects of the present invention may provide, for example, a CMOS phase lock loop that may include, for example, oscillator means, mixer means and detector means. The oscillator means may generate, for example, a first signal having a tunable frequency and may include, for example, tuning means that tune the frequency of the first signal. The mixer means may mix, for example, the first signal with a second signal to produce a mixed signal. The detector means may detect, for example, a phase difference between the mixed signal and an input signal, and may generate, for example, an error signal which is a function of the phase difference. The tuning means may be responsive, for example, to the error signal.

ISSUES FOR REVIEW

Whether claims 1-6, 8-13 and 15-20 are unpatentable under 35 U.S.C. § 103(a) as being obvious over United States Patent No. 5,686,867 to Pantas Sutardja et al. ("Sutardja") in view of United States Patent No. 5,341,110 to Benedict J. Nardi ("Nardi").

Whether claims 7, 14 and 21 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Sutardja in view of Nardi, and further in view of United States Patent No. 4,270,206 to William C. Hughes ("Hughes").

GROUPING OF CLAIMS

Claims 1-21 do not stand or fall together.

Group I.	Claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20
Group II.	Claim 3
Group III.	Claim 10
Group IV.	Claim 4
Group V.	Claim 11

Group VI. Claim 18
Group VII. Claim 7
Group VIII. Claim 14
Group IX. Claim 21

ARGUMENT

I. Group I: Claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20

Claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 stand rejected as being obvious over Sutardja in view of Nardi. Appellants respectfully request that the Board reverse the rejection.

The Examiner carries the responsibility of making sure that the standard of patentability enunciated by the United States Supreme Court is applied in each and every case. See, e.g., M.P.E.P. § 2141; and Graham v. John Deere, 383 U.S. 1, 148 U.S.P.Q. 459 (1966).

The Examiner bears the burden of presenting a *prima facie* case of obviousness. If the Examiner does not produce a *prima facie* case of obviousness, Appellants are under no obligation to submit evidence of nonobviousness. See, e.g., M.P.E.P. § 2142.

Appellants respectfully submit that the claims are patentable over Sutardja in view of Nardi because Sutardja and Nardi were improperly combined. Accordingly, not even a *prima facie* case of obviousness has been presented by the Examiner.

M.P.E.P. § 2145(X)(D)(2) states that "[i]t is improper to combine references where the references teach away from their combination." M.P.E.P. § 2145(X)(D)(2) (citing, e.g., In re Grasselli, 713 F.2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983)). Appellants respectfully submit that Sutardja and Nardi were improperly combined.

Nardi teaches a YIG tuned resonator having inductive coils and Nardi specifically disparages methods of resonator tuning that do not rely upon inductive coils. Appellants respectfully draw the attention of the Board to Nardi which states that "[m]ethods of resonator tuning not relying upon inductive coils (e.g., those using varactor diodes), have tended to degrade phase noise performance by inducing non-linear tuning characteristics or by lowering the oscillator Q". Nardi at col. 2, lines 18-22. On the other hand, Sutardja teaches away from Nardi by not relying upon inductive coils for resonator tuning.

Instead, Sutardja teaches methods for resonator tuning that do no rely upon inductive coils such as, for example, variable resistances and variable bias currents. See, e.g., voltage controlled oscillators (VCOs) illustrated in Sutardja at FIGS. 2-5 and 9-11. According to Nardi, Sutardja teaches method for resonator tuning that degrade phase noise performance.

The object of the invention described in Nardi and the reason for combining Sutardja in view of Nardi according to the Examiner is to increase loop bandwidth in a phase-locking oscillator. However, the reason for increasing loop bandwidth is to improve phase noise performance which Sutardja is teaching away from according to the teachings of Nardi. Thus, not only does Sutardja teach away from the teachings of Nardi, but the effect of the teachings of Sutardja, according to Nardi, is to teach away from the very object of the invention described in Nardi and to teach away from the motivation for combining Sutardja and Nardi as alleged by the Examiner.

Furthermore, Nardi teaches away from Sutardja. Nardi requires a YIG resonator because of the desirable phase noise characteristics of YIG tuned oscillators and because of the high quality factors (Q). See, e.g., Nardi at col. 1, lines 22-27. As discussed above, Nardi also teaches that the YIG tuned oscillator should rely upon inductive coils, (as opposed to varactor diodes, for example), so as to not degrade phase noise performance of the YIG tune oscillator. See, e.g., Nardi at col. 2, lines 19-23. However, the requirement of inductive coil discrete components teach away from a "monolithic CMOS phase-lock loop (PLL) circuit" as taught by Sutardja. See, e.g., Sutardja at the Abstract. By requiring inductive coils, Nardi teaches away from CMOS technology and CMOS integration as taught by Sutardja.

Thus, Nardi not only teaches away from the monolithic CMOS PLL circuit as taught by Sutardja, but Nardi also teaches away from a "complimentary metal oxide semiconductor (CMOS) phase lock loop" as set forth in independent claims 1, 8 and 15. M.P.E.P. § 2145(X)(D)(1) states that "[a] prior art reference that 'teaches away' from the claimed invention is a significant factor to be considered in determining obviousness". M.P.E.P. § 2145(X)(D)(1) (citing, e.g., In re Gurley, 27 F.3d 551, 554, 31 U.S.P.Q.2d 1130, 1132 (Fed. Cir. 1994)).

Sutardja teaches that "[m]any conventional VCOs, such as those described later herein in conjunction with FIGS. 2, 3 and 4 do no have supply rejection capability and thus are susceptible to supply noise induced jitter." Sutardja at col. 1, lines 27-30. As can be seen in Sutardja at FIGS. 2 and 4, for example, ripples in the power supply VDD directly affect that oscillation frequency of the VCO, thereby resulting in supply noise induced jitter. Sutardja states that "[i]t is an object of the invention to provide a VCO circuit with substantially higher level of supply rejection for lowering the jitter of the VCO." Sutardja at col. 1, lines 55-57. Nardi teaches away from the object of the invention of Sutardja by exposing a coarse tuning input of the YIG resonator 108 to supply noise induced jitter. In Nardi at FIG. 5A, the YIG coil driver is directly exposed to power supply V_{DD} which directly affects the current output by transistor 254. Nardi states that "[t]he oscillation frequency of the coarse-tune coil of the YIG tuned oscillator 108 is proportional to the current supplied thereto by the transistor 254". Nardi at col. 5, lines 28-30. Thus, supply noise jitter shows up as current output jitter in the output of transistor 254 which, in turn, shows up as frequency jitter in the YIG tuned oscillator 108. Thus, Nardi teaches away from the very object of the invention as described in Sutardja.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained based on the combination of Sutardja and Nardi. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20.

II. Group II: Claim 3

Claim 3 stands rejected as being obvious over Sutardja in view of Nardi. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section II with respect to claim 3.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi.

In addition, claim 3 recites "a bandpass filter to filter the mixed signal before being applied to the phase detector". In the Office Action Made Final, the Examiner admits that "Sutardja fails to disclose a bandpass filter to filter the mixed signal before

being applied to the phase detector". Office Action Made Final of April 22, 2005 at page 3. In the Advisory Action, the Examiner offers no less than two separate allegations as to the teachings of Sutardja in view of Nardi with respect to the bandpass filter as set forth in claim 3. Appellants respectfully submit that Nardi does not make up for the teaching deficiencies of Sutardja.

First, the Examiner alleges that Nardi teaches in FIG. 4 that low frequency path loop filter 190 or high frequency path loop filter 194 is a bandpass filter. In support of such an allegation, the Examiner cites Nardi at col. 4, lines 39-62 and col. 3, lines 46-61. With respect to low frequency path loop filter 190 and high frequency loop filter 194, in the cited text, Nardi states that "[t]he loop filters 190 and 194 serve to close low-frequency and high-frequency feedback paths P_{low} and P_{high}, respectively, within the oscillator circuits 150". Nardi at col. 4, lines 41-43. Thus, Nardi in the cited text only teaches that filters 190 and 194 close feedback paths and, by their names, suggest a low-frequency feedback path or a high-frequency feedback path. However, there is no teaching that filters 190 or 194 are bandpass filters.

Second, the Examiner alleges that bandpass filter 270 in Nardi at FIG. 5b is the bandpass filter as set forth in claim 3. However, this is not the case. Bandpass filter 270 does not filter the mixed signal before being applied to the phase detector. Instead, the bandpass filter 270 filters the harmonics generated by line generator 266 *before* even reaching mixer 274. Thus, Nardi does not teach a bandpass filter to filter the mixed signal.

For at least the above reasons, it is respectfully submitted that Sutardja and Nardi, individually or combined, do not teach each and every element as set forth in claim 3. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 3.

III. Group III: Claim 10

Claim 10 stands rejected as being obvious over Sutardja in view of Nardi. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section III with respect to claim 10.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi.

In addition, claim 10 depends from claim 8. Claim 8 recites "a phase detector having a first input coupled to the mixer". Claim 10 recites "a bandpass filter coupled between the mixer and the first input of the phase detector". In the Office Action Made Final, the Examiner admits that "Sutardja fails to disclose a bandpass filter coupled between the mixer and the first input of the phase detector". Office Action Made Final of April 22, 2005 at page 6. In the Advisory Action, the Examiner offers no less than two separate allegations as to the teachings of Sutardja in view of Nardi with respect to the bandpass filter as set forth in claim 10. Appellants respectfully submit that Nardi does not make up for the teaching deficiencies of Sutardja.

First, the Examiner alleges that Nardi teaches in FIG. 4 that low frequency path loop filter 190 or high frequency path loop filter 194 is a bandpass filter. In support of such an allegation, the Examiner cites Nardi at col. 4, lines 39-62 and col. 3, lines 46-61. With respect to low frequency path loop filter 190 and high frequency loop filter 194, in the cited text, Nardi states that "[t]he loop filters 190 and 194 serve to close low-frequency and high-frequency feedback paths P_{low} and P_{high}, respectively, within the oscillator circuits 150". Nardi at col. 4, lines 41-43. Thus, Nardi in the cited text only teaches that filters 190 and 194 close feedback paths and, by their names, suggest a low-frequency feedback path or a high-frequency feedback path. However, there is no teaching that filters 190 or 194 are bandpass filters.

Second, the Examiner alleges that bandpass filter 270 in Nardi at FIG. 5b is the bandpass filter as set forth in claim 10. However, this is not the case. Bandpass filter 270 (FIG. 5B) is not coupled between mixer 274 (FIG. 5B) and the first input of phase detector 172 (FIG. 5A). Thus, Nardi does not teach a bandpass filter coupled between the

mixer and the first input of the phase detector that is logically consistent with claims 8 and 10.

For at least the above reasons, it is respectfully submitted that Sutardja and Nardi, individually or combined, do not teach each and every element as set forth in claim 10. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 10.

IV. Group IV: Claim 4

Claim 4 stands rejected as being obvious over Sutardja in view of Nardi. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section IV with respect to claim 4.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 4.

Claim 4 depends from claim 3. The arguments made in Section II with respect to claim 3 are made here in Section IV with respect to claim 4.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 4.

In addition, claim 4 recites "a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector". The Examiner has already admitted that "Sutardja fails to disclose a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector". Office Action Made Final of April 22, 2005 at page 4. The Board would expect, as would Appellants, that the Examiner would next explain how Nardi teaches a limiter as set forth in claim 4. Instead, the Examiner cut and paste the same summary of Nardi, regardless of claim language, that was also recited verbatim for claims 1, 3, 8, 10, 11, 15 and 17. Appellants respectfully draw the attention of the Board to the fact that the ubiquitous Nardi summary does not set forth a *prima facie* case of obviousness as to the limiter as set forth in claim 4. In fact, the word "limiter" is no where to be found in the oft-repeated Nardi summary.

Furthermore, as far back as the Response of June 1, 2004 at pages 3 and 4, Appellants have respectfully and specifically requested that the Examiner identify the limiter in Nardi. In the Reply After Final Rejection of June 22, 2005 at pages 2 and 3, in centered, bold lettering, Appellants again respectfully requested that the Examiner identify the limiter in Nardi. At no time during the prosecution of the present application has the Examiner ever once identified the limiter in Nardi. Appellants respectfully submit that the Examiner has failed in his burden to present a *prima facie* case of obviousness. Since the Examiner has not produce a *prima facie* case of obviousness, Appellants are under no obligation to submit further evidence of nonobviousness. See, e.g., M.P.E.P. § 2142.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 4.

V. Group V: Claim 11

Claim 11 stands rejected as being obvious over Sutardja in view of Nardi. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section V with respect to claim 11.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 11.

Claim 11 depends from claim 10. The arguments made in Section III with respect to claim 10 are made here in Section V with respect to claim 11.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 11.

In addition, claim 11 recites "a limiter coupled between the bandpass filter and the first input of the phase detector". The Examiner has already admitted that "Sutardja fails to disclose a limiter coupled between the bandpass filter and the first input of the phase detector". Office Action Made Final of April 22, 2005 at page 7. The Board would expect, as would Appellants, that the Examiner would next explain how Nardi teaches a

limiter as set forth in claim 11. Instead, the Examiner cut and paste the same summary of Nardi, regardless of claim language, that was also recited verbatim for claims 1, 3, 4, 8, 10, 15 and 17. Appellants respectfully draw the attention of the Board to the fact that the ubiquitous Nardi summary does not set forth a *prima facie* case of obviousness as to the limiter as set forth in claim 11. In fact, the word "limiter" is no where to be found in the oft-repeated Nardi summary.

Furthermore, as far back as the Response of June 1, 2004 at pages 3 and 4, Appellants have respectfully and specifically requested that the Examiner identify a limiter in Nardi. In the Reply After Final Rejection of June 22, 2005 at pages 2 and 3, in centered, bold lettering, Appellants again respectfully requested that the Examiner identify a limiter in Nardi. At no time during the prosecution of the present application has the Examiner ever once identified a limiter in Nardi. Appellants respectfully submit that the Examiner has failed in his burden to present a *prima facie* case of obviousness. Since the Examiner has not produce a *prima facie* case of obviousness, Appellants are under no obligation to submit further evidence of nonobviousness. See, e.g., M.P.E.P. § 2142.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 11.

VI. Group VI: Claim 18

Claim 18 stands rejected as being obvious over Sutardja in view of Nardi. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section VI with respect to claim 18.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 18.

In addition, claim 18 recites "means for limiting the filtered mixed signal from the filter means before being applied to the detector means". As already documented above with respect to claims 4 and 11, the oft-repeated Nardi summary does not present a *prima*

facie case of obviousness with respect to a limiter as set forth in claim 18. In fact, the word "limiter" is no where to be found in the oft-repeated Nardi summary.

As documented above, despite repeated requests that the Examiner identify a limiter in Nardi, it is a matter of record that, at no time during the prosecution of the present application, has the Examiner identified a limiter in Nardi. Appellants respectfully submit that the Examiner has failed in his burden to present a *prima facie* case of obviousness. Since the Examiner has not produce a *prima facie* case of obviousness, Appellants are under no obligation to submit further evidence of nonobviousness. See, e.g., M.P.E.P. § 2142.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 18.

VII. Group VII: Claim 7

Claim 7 stands rejected as being obvious over Sutardja in view of Nardi, and further in view of Hughes. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section VII with respect to claim 7.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on the combination of Sutardja and Nardi with respect to claim 7.

In addition, claim 7 recites "a bandpass filter to filter the mixed signal before being applied to the phase detector". Since at least these elements of claim 7 are the same as the elements recited above with respect to claim 3, the arguments made in Section II with respect to claim 3 are made here in Section VII with respect to claim 7. In addition, Hughes does not make up for the teaching deficiencies of Sutardja in view of Nardi. Hughes teaches that bandpass filter-amplifier means 74 is connected to receiver input 16a which is connected to the transmission medium, which in Hughes is power line 11. Thus, the incoming signal is immediately bandpass filtered before any mixing occurs. See, e.g., Hughes at FIG. 1A and 1C.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 7.

In addition, claim 7 recites "a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector". Since at least these elements of claim 7 are the same as the elements recited above with respect to claim 4, the arguments made in Section IV with respect to claim 4 are made here in Section VII with respect to claim 7. In addition, Hughes does not make up for the teaching deficiencies of Sutardja in view of Nardi. Hughes is silent as a limiter to limit a filtered mixed signal before being applied to a phase detector.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 7.

Furthermore, Appellants respectfully submit that Hughes teaches away from the alleged motivation for combining Sutardja, Nardi and Hughes which, according to the Examiner, "to employ a phase modulator in conjunction with a resonator in order to realize a phase locking oscillator circuit having a loop bandwidth broader than that of existing oscillator circuits". Office Action Made Final of April 22, 2005 at page 12. Nardi at FIG. 2 shows that the reason for expanding the loop bandwidth is because as phase noise of the reference oscillator 18 improves, to take advantage of the favorable phase noise plot as illustrated in FIG. 2, the loop bandwidth needs to be expanded beyond at least 10^6 radians. Compare this with Hughes, which is a power line communications system that operates at 60 Hz. To incorporate bandpass filter-amplifier means 74 of Hughes would effectively decrease loop bandwidth if the bandpass filter-amplifier means 74 were inserted into the Sutardja circuit modified by the Nardi circuit.

Appellants respectfully submit that one of ordinary skill in the art would not look to Hughes which operates at a system-wide frequency of 60 Hz for teachings to expand loop bandwidth beyond at least 10^6 radians. Furthermore, since the bandpass filter-amplifier means 74 is not part of phase lock loop 64 found in Hughes at FIG. 1D,

Appellants further challenge the motivation for taking bandpass filter-amplifier means 74 of Hughes and sticking it in a phase lock loop modified by Sutardja in view of Nardi as suggested by the Examiner.

Appellants further submit that Sutardja teaches power supply rejection capabilities to reduce phase noise and jitter as previously described above. Yet, Hughes teaches directly receiving signals from a power line which is an extremely noisy power supply. Respectfully, Hughes and Sutardja teach away from each other and should not be combined.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 7.

VIII. Group VIII: Claim 14

Claim 14 stands rejected as being obvious over Sutardja in view of Nardi, and further in view of Hughes. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section VIII with respect to claim 14.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on the combination of Sutardja and Nardi with respect to claim 14.

In addition, claim 14 recites "a limiter coupled between the bandpass filter and the first input of the phase detector". Since at least these elements of claim 14 are the same as the elements recited above with respect to claim 11, the arguments made in Section V with respect to claim 11 are made here in Section VIII with respect to claim 14. In addition, Hughes does not make up for the teaching deficiencies of Sutardja in view of Nardi. Hughes is silent as a limiter to limit a filtered mixed signal before being applied to a phase detector.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the

obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 14.

Furthermore, Appellants respectfully submit that Hughes teaches away from the alleged motivation for combining Sutardja, Nardi and Hughes which, according to the Examiner, "to employ a phase modulator in conjunction with a resonator in order to realize a phase locking oscillator circuit having a loop bandwidth broader than that of existing oscillator circuits". Office Action Made Final of April 22, 2005 at page 12. Nardi at FIG. 2 shows that the reason for expanding the loop bandwidth is because as phase noise of the reference oscillator 18 improves, to take advantage of the favorable phase noise plot as illustrated in FIG. 2, the loop bandwidth needs to be expanded beyond at least 10^6 radians. Compare this with Hughes, which is a power line communications system that operates at 60 Hz. To incorporate bandpass filter-amplifier means 74 of Hughes would effectively decrease loop bandwidth if the bandpass filter-amplifier means 74 were inserted into the Sutardja circuit modified by the Nardi circuit.

Appellants respectfully submit that one of ordinary skill in the art would not look to Hughes which operates at a system-wide frequency of 60 Hz for teachings to expand loop bandwidth beyond at least 10^6 radians. Furthermore, since the bandpass filter-amplifier means 74 is not part of phase lock loop 64 found in Hughes at FIG. 1D, Appellants further challenge the motivation for taking bandpass filter-amplifier means 74 of Hughes and sticking it in a phase lock loop modified by Sutardja in view of Nardi as suggested by the Examiner.

Appellants further submit that Sutardja teaches power supply rejection capabilities to reduce phase noise and jitter as previously described above. Yet, Hughes teaches directly receiving signals from a power line which is an extremely noisy power supply. Respectfully, Hughes and Sutardja teach away from each other and should not be combined.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 14.

IX. Group IX: Claim 21

Claim 21 stands rejected as being obvious over Sutardja in view of Nardi, and further in view of Hughes. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section IX with respect to claim 21.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on the combination of Sutardja and Nardi with respect to claim 21.

In addition, claim 21 recites "means for limiting the filtered mixed signal from the filter means before being applied to the detector means". Since at least these elements of claim 21 are the same as the elements recited above with respect to claim 18, the arguments made in Section VI with respect to claim 18 are made here in Section IX with respect to claim 21.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 21.

Furthermore, Appellants respectfully submit that Hughes teaches away from the alleged motivation for combining Sutardja, Nardi and Hughes which, according to the Examiner, "to employ a phase modulator in conjunction with a resonator in order to realize a phase locking oscillator circuit having a loop bandwidth broader than that of existing oscillator circuits". Office Action Made Final of April 22, 2005 at page 12. Nardi at FIG. 2 shows that the reason for expanding the loop bandwidth is because as phase noise of the reference oscillator 18 improves, to take advantage of the favorable phase noise plot as illustrated in FIG. 2, the loop bandwidth needs to be expanded beyond at least 10^6 radians. Compare this with Hughes, which is a power line communications system that operates at 60 Hz. As alleged by the Examiner, to incorporate bandpass filter-amplifier means 74 of Hughes would effectively decrease loop bandwidth if the bandpass filter-amplifier means 74 were inserted into the Sutardja circuit modified by the Nardi circuit.

Appellants respectfully submit that one of ordinary skill in the art would not look to Hughes which operates at a system-wide frequency of 60 Hz for teachings to expand loop bandwidth beyond at least 10^6 radians. Furthermore, since the bandpass filter-amplifier means 74 (which the Examiner alleges is filter means with respect to claim 21) is not part of phase lock loop 64 found in Hughes at FIG. 1D, Appellants further challenge the motivation for taking bandpass filter-amplifier means 74 of Hughes and sticking it in a phase lock loop modified by Sutardja in view of Nardi as suggested by the Examiner.

Appellants further submit that Sutardja teaches power supply rejection capabilities to reduce phase noise and jitter as previously described above. Yet, Hughes teaches directly receiving signals from a power line which is an extremely noisy power supply. Respectfully, Hughes and Sutardja teach away from each other and should not be combined.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 21.

X. Conclusion

For the foregoing reasons, claims 1-21 are patentable over the alleged prior art of record. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: October 25, 2005

Respectfully submitted,

Michael T. Cruz

Michael T. Cruz
Registration No. 44,636

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
Telephone: (312) 775-8084
Facsimile: (312) 775-8100

APPENDIX

The following claims are involved in this appeal:

1. A complimentary metal oxide semiconductor (CMOS) phase lock loop, comprising:

an oscillator having a tuning input, and an output with a tunable frequency responsive to the tuning input;

a mixer to mix the oscillator output with a second signal to produce a mixed signal; and

a phase detector outputting an error signal which is a function of a phase difference between the mixed signal and an input signal, the error signal being applied to the tuning input.

2. The CMOS phase lock loop of claim 1 wherein the oscillator comprises a voltage controlled oscillator, the tuning input being responsive to a voltage of the error signal.

3. The CMOS phase lock loop of claim 1 further comprising a bandpass filter to filter the mixed signal before being applied to the phase detector, the filtered mixed signal comprising a difference frequency between the tuned frequency of the oscillator output and a frequency of the second signal.

4. The CMOS phase lock loop of claim 3 further comprising a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector.

5. The CMOS phase lock loop of claim 1 further comprising a charge pump disposed between the phase detector and the oscillator.

6. The CMOS phase lock loop of claim 1 further comprising a loop filter disposed between the phase detector and the oscillator.

7. The CMOS phase lock loop of claim 1 wherein the oscillator comprises a voltage controlled oscillator, the tuning input being responsive to a voltage of the error signal, the CMOS phase lock loop further comprising a bandpass filter to filter the mixed signal before being applied to the phase detector, the filtered mixed signal comprising a difference frequency between the tuned frequency of the oscillator output and a frequency of the second signal, a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector, a charge pump disposed between the phase detector and the oscillator, and a loop filter disposed between the charge pump and the oscillator.

8. A complimentary metal oxide semiconductor (CMOS) phase lock loop, comprising:

a tunable oscillator having a tuning input;

a mixer coupled the oscillator; and

a phase detector having a first input coupled to the mixer, a second input adapted to receive an input signal, and an output coupled to the tuning input.

9. The CMOS phase lock loop of claim 8 wherein the oscillator comprises a voltage controlled oscillator.

10. The CMOS phase lock loop of claim 8 further comprising a bandpass filter coupled between the mixer and the first input of the phase detector.

11. The CMOS phase lock loop of claim 10 further comprising a limiter coupled between the bandpass filter and the first input of the phase detector.

12. The CMOS phase lock loop of claim 8 further comprising a charge pump coupled between the phase detector output and the tuning input of the oscillator.

13. The CMOS phase lock loop of claim 8 further comprising a loop filter coupled between the phase detector output and the tuning input of the oscillator.

14. The CMOS phase lock loop of claim 8 wherein the oscillator comprises a voltage controlled oscillator, the CMOS phase lock loop further comprising a bandpass filter coupled to the mixer, a limiter coupled between the bandpass filter and the first input of the phase detector, a charge pump coupled to the phase detector output, and a loop filter coupled between the charge pump and the tuning input of the oscillator.

15. A complimentary metal oxide semiconductor (CMOS) phase lock loop, comprising:

oscillator means for generating a first signal having a tunable frequency, the oscillating means comprising tuning means for tuning the frequency of the first signal;

mixer means for mixing the first signal with a second signal to produce a mixed signal; and

detector means for detecting a phase difference between the mixed signal and an input signal, and generating an error signal which is a function of the phase difference, the tuning means being responsive to the error signal.

16. The CMOS phase lock loop of claim 15 wherein the oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal.

17. The CMOS phase lock loop of claim 15 further comprising filter means for filtering the mixed signal before being applied to the detector means, the filtered mixed signal comprising a difference frequency between the tuned frequency of the first signal and a frequency of the second signal.

18. The CMOS phase lock loop of claim 17 further comprising means for limiting the filtered mixed signal from the filter means before being applied to the detector means.

19. The CMOS phase lock loop of claim 15 further comprising means for sourcing current to the tuning means responsive to the error signal.

20. The CMOS phase lock loop of claim 15 further comprising means for filtering the error signal from the detecting means before being applied to the tuning means.

21. The CMOS phase lock loop of claim 15 wherein the oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal, the CMOS phase lock loop further comprising filter means for filtering the mixed signal before being applied to the detector means, the filtered mixed signal comprising a difference frequency between the tuned frequency of the first signal and a frequency of the second signal, means for limiting the filtered mixed signal from the filter means before being applied to the detector means, current means for sourcing current to the tuning means responsive to the error signal, and means for filtering the current sourced error signal from the current means before being applied to the tuning means.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. 15258US08

In the Application of:

Ahmadreza Rofougaran et al.

U.S. Serial No.: 09/698,498

Filed: October 27, 2000

For: ADAPTIVE RADIO TRANSCEIVER WITH NOISE SUPPRESSION

Examiner: Marceau Milord

Group Art Unit: 2682

Confirmation No.: 3857

Certificate of Facsimile Transmission

I hereby certify that this correspondence is being sent via facsimile transmission to the United States Patent and Trademark Office at (571) 273-8300 on October 25, 2005.

Michael T. Cruz
Michael T. Cruz
Reg. No. 44,636

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Notice of Appeal was received by the United States Patent and Trademark Office on July 25, 2005 for the above-identified patent application. A Petition for a One-Month Extension has been enclosed, thereby extending the deadline for filing an Appeal Brief in support of the Notice of Appeal to October 25, 2005.

REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 16215 Alton Parkway, Irvine, California 92618-3616, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment filed with the present application and recorded on Reel 011785, Frame 0092.

RELATED APPEALS AND INTERFERENCES

There are currently no appeals pending regarding related applications.

STATUS OF THE CLAIMS

Claims 1-21 are pending in the present application. Pending claims 1-21 have been rejected under 35 U.S.C. § 103(a) and are the subject of this appeal.

STATUS OF THE AMENDMENTS

There are no amendments pending in the present application.

SUMMARY OF THE INVENTION

Some embodiments according to some aspects of the present invention may provide, for example, a complimentary metal oxide semiconductor (CMOS) phase lock loop that may include, for example, an oscillator, a mixer and a phase detector. The oscillator may have, for example, a tuning input and an output with a tunable frequency responsive to the tuning input. The mixer may mix, for example, the oscillator output with a second signal to produce a mixed signal. The phase detector may output, for example, an error signal which is a function of a phase difference between the mixed signal and an input signal. The error signal may be applied, for example, to the tuning input.

Some embodiment according to some aspects of the present invention may provide, for example, a CMOS phase lock loop that may include, for example, a tunable

oscillator, a mixer and a phase detector. The tunable oscillator may have, for example, a tuning input. The mixer may be coupled, for example, to the oscillator. The phase detector may have, for example, a first input coupled to the mixer, a second input adapted to receive an input signal, and an output coupled to the tuning input.

Some embodiments according to some aspects of the present invention may provide, for example, a CMOS phase lock loop that may include, for example, oscillator means, mixer means and detector means. The oscillator means may generate, for example, a first signal having a tunable frequency and may include, for example, tuning means that tune the frequency of the first signal. The mixer means may mix, for example, the first signal with a second signal to produce a mixed signal. The detector means may detect, for example, a phase difference between the mixed signal and an input signal, and may generate, for example, an error signal which is a function of the phase difference. The tuning means may be responsive, for example, to the error signal.

ISSUES FOR REVIEW

Whether claims 1-6, 8-13 and 15-20 are unpatentable under 35 U.S.C. § 103(a) as being obvious over United States Patent No. 5,686,867 to Pantas Sutardja et al. ("Sutardja") in view of United States Patent No. 5,341,110 to Benedict J. Nardi ("Nardi").

Whether claims 7, 14 and 21 are unpatentable under 35 U.S.C. § 103(a) as being obvious over Sutardja in view of Nardi, and further in view of United States Patent No. 4,270,206 to William C. Hughes ("Hughes").

GROUPING OF CLAIMS

Claims 1-21 do not stand or fall together.

Group I.	Claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20
Group II.	Claim 3
Group III.	Claim 10
Group IV.	Claim 4
Group V.	Claim 11

Group VI.	Claim 18
Group VII.	Claim 7
Group VIII.	Claim 14
Group IX.	Claim 21

ARGUMENT

I. Group I: Claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20

Claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 stand rejected as being obvious over Sutardja in view of Nardi. Appellants respectfully request that the Board reverse the rejection.

The Examiner carries the responsibility of making sure that the standard of patentability enunciated by the United States Supreme Court is applied in each and every case. See, e.g., M.P.E.P. § 2141; and Graham v. John Deere, 383 U.S. 1, 148 U.S.P.Q. 459 (1966).

The Examiner bears the burden of presenting a *prima facie* case of obviousness. If the Examiner does not produce a *prima facie* case of obviousness, Appellants are under no obligation to submit evidence of nonobviousness. See, e.g., M.P.E.P. § 2142.

Appellants respectfully submit that the claims are patentable over Sutardja in view of Nardi because Sutardja and Nardi were improperly combined. Accordingly, not even a *prima facie* case of obviousness has been presented by the Examiner.

M.P.E.P. § 2145(X)(D)(2) states that "[i]t is improper to combine references where the references teach away from their combination." M.P.E.P. § 2145(X)(D)(2) (citing, e.g., In re Grasselli, 713 F.2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983)). Appellants respectfully submit that Sutardja and Nardi were improperly combined.

Nardi teaches a YIG tuned resonator having inductive coils and Nardi specifically disparages methods of resonator tuning that do not rely upon inductive coils. Appellants respectfully draw the attention of the Board to Nardi which states that "[m]ethods of resonator tuning not relying upon inductive coils (e.g., those using varactor diodes), have tended to degrade phase noise performance by inducing non-linear tuning characteristics or by lowering the oscillator Q". Nardi at col. 2, lines 18-22. On the other hand, Sutardja teaches away from Nardi by not relying upon inductive coils for resonator tuning.

Instead, Sutardja teaches methods for resonator tuning that do no rely upon inductive coils such as, for example, variable resistances and variable bias currents. See, e.g., voltage controlled oscillators (VCOs) illustrated in Sutardja at FIGS. 2-5 and 9-11. According to Nardi, Sutardja teaches method for resonator tuning that degrade phase noise performance.

The object of the invention described in Nardi and the reason for combining Sutardja in view of Nardi according to the Examiner is to increase loop bandwidth in a phase-locking oscillator. However, the reason for increasing loop bandwidth is to improve phase noise performance which Sutardja is teaching away from according to the teachings of Nardi. Thus, not only does Sutardja teach away from the teachings of Nardi, but the effect of the teachings of Sutardja, according to Nardi, is to teach away from the very object of the invention described in Nardi and to teach away from the motivation for combining Sutardja and Nardi as alleged by the Examiner.

Furthermore, Nardi teaches away from Sutardja. Nardi requires a YIG resonator because of the desirable phase noise characteristics of YIG tuned oscillators and because of the high quality factors (Q). See, e.g., Nardi at col. 1, lines 22-27. As discussed above, Nardi also teaches that the YIG tuned oscillator should rely upon inductive coils, (as opposed to varactor diodes, for example), so as to not degrade phase noise performance of the YIG tune oscillator. See, e.g., Nardi at col. 2, lines 19-23. However, the requirement of inductive coil discrete components teach away from a "monolithic CMOS phase-lock loop (PLL) circuit" as taught by Sutardja. See, e.g., Sutardja at the Abstract. By requiring inductive coils, Nardi teaches away from CMOS technology and CMOS integration as taught by Sutardja.

Thus, Nardi not only teaches away from the monolithic CMOS PLL circuit as taught by Sutardja, but Nardi also teaches away from a "complimentary metal oxide semiconductor (CMOS) phase lock loop" as set forth in independent claims 1, 8 and 15. M.P.E.P. § 2145(X)(D)(1) states that "[a] prior art reference that 'teaches away' from the claimed invention is a significant factor to be considered in determining obviousness". M.P.E.P. § 2145(X)(D)(1) (citing, e.g., In re Gurley, 27 F.3d 551, 554, 31 U.S.P.Q.2d 1130, 1132 (Fed. Cir. 1994)).

Sutardja teaches that "[m]any conventional VCOs, such as those described later herein in conjunction with FIGS. 2, 3 and 4 do no have supply rejection capability and thus are susceptible to supply noise induced jitter." Sutardja at col. 1, lines 27-30. As can be seen in Sutardja at FIGS. 2 and 4, for example, ripples in the power supply VDD directly affect that oscillation frequency of the VCO, thereby resulting in supply noise induced jitter. Sutardja states that "[i]t is an object of the invention to provide a VCO circuit with substantially higher level of supply rejection for lowering the jitter of the VCO." Sutardja at col. 1, lines 55-57. Nardi teaches away from the object of the invention of Sutardja by exposing a coarse tuning input of the YIG resonator 108 to supply noise induced jitter. In Nardi at FIG. 5A, the YIG coil driver is directly exposed to power supply V_{DD} which directly affects the current output by transistor 254. Nardi states that "[t]he oscillation frequency of the coarse-tune coil of the YIG tuned oscillator 108 is proportional to the current supplied thereto by the transistor 254". Nardi at col. 5, lines 28-30. Thus, supply noise jitter shows up as current output jitter in the output of transistor 254 which, in turn, shows up as frequency jitter in the YIG tuned oscillator 108. Thus, Nardi teaches away from the very object of the invention as described in Sutardja.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained based on the combination of Sutardja and Nardi. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20.

II. Group II: Claim 3

Claim 3 stands rejected as being obvious over Sutardja in view of Nardi. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section II with respect to claim 3.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi.

In addition, claim 3 recites "a bandpass filter to filter the mixed signal before being applied to the phase detector". In the Office Action Made Final, the Examiner admits that "Sutardja fails to disclose a bandpass filter to filter the mixed signal before

being applied to the phase detector". Office Action Made Final of April 22, 2005 at page 3. In the Advisory Action, the Examiner offers no less than two separate allegations as to the teachings of Sutardja in view of Nardi with respect to the bandpass filter as set forth in claim 3. Appellants respectfully submit that Nardi does not make up for the teaching deficiencies of Sutardja.

First, the Examiner alleges that Nardi teaches in FIG. 4 that low frequency path loop filter 190 or high frequency path loop filter 194 is a bandpass filter. In support of such an allegation, the Examiner cites Nardi at col. 4, lines 39-62 and col. 3, lines 46-61. With respect to low frequency path loop filter 190 and high frequency loop filter 194, in the cited text, Nardi states that "[t]he loop filters 190 and 194 serve to close low-frequency and high-frequency feedback paths P_{low} and P_{high}, respectively, within the oscillator circuits 150". Nardi at col. 4, lines 41-43. Thus, Nardi in the cited text only teaches that filters 190 and 194 close feedback paths and, by their names, suggest a low-frequency feedback path or a high-frequency feedback path. However, there is no teaching that filters 190 or 194 are bandpass filters.

Second, the Examiner alleges that bandpass filter 270 in Nardi at FIG. 5b is the bandpass filter as set forth in claim 3. However, this is not the case. Bandpass filter 270 does not filter the mixed signal before being applied to the phase detector. Instead, the bandpass filter 270 filters the harmonics generated by line generator 266 *before* even reaching mixer 274. Thus, Nardi does not teach a bandpass filter to filter the mixed signal.

For at least the above reasons, it is respectfully submitted that Sutardja and Nardi, individually or combined, do not teach each and every element as set forth in claim 3. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 3.

III. Group III: Claim 10

Claim 10 stands rejected as being obvious over Sutardja in view of Nardi. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section III with respect to claim 10.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi.

In addition, claim 10 depends from claim 8. Claim 8 recites "a phase detector having a first input coupled to the mixer". Claim 10 recites "a bandpass filter coupled between the mixer and the first input of the phase detector". In the Office Action Made Final, the Examiner admits that "Sutardja fails to disclose a bandpass filter coupled between the mixer and the first input of the phase detector". Office Action Made Final of April 22, 2005 at page 6. In the Advisory Action, the Examiner offers no less than two separate allegations as to the teachings of Sutardja in view of Nardi with respect to the bandpass filter as set forth in claim 10. Appellants respectfully submit that Nardi does not make up for the teaching deficiencies of Sutardja.

First, the Examiner alleges that Nardi teaches in FIG. 4 that low frequency path loop filter 190 or high frequency path loop filter 194 is a bandpass filter. In support of such an allegation, the Examiner cites Nardi at col. 4, lines 39-62 and col. 3, lines 46-61. With respect to low frequency path loop filter 190 and high frequency loop filter 194, in the cited text, Nardi states that "[t]he loop filters 190 and 194 serve to close low-frequency and high-frequency feedback paths P_{low} and P_{high}, respectively, within the oscillator circuits 150". Nardi at col. 4, lines 41-43. Thus, Nardi in the cited text only teaches that filters 190 and 194 close feedback paths and, by their names, suggest a low-frequency feedback path or a high-frequency feedback path. However, there is no teaching that filters 190 or 194 are bandpass filters.

Second, the Examiner alleges that bandpass filter 270 in Nardi at FIG. 5b is the bandpass filter as set forth in claim 10. However, this is not the case. Bandpass filter 270 (FIG. 5B) is not coupled between mixer 274 (FIG. 5B) and the first input of phase detector 172 (FIG. 5A). Thus, Nardi does not teach a bandpass filter coupled between the

mixer and the first input of the phase detector that is logically consistent with claims 8 and 10.

For at least the above reasons, it is respectfully submitted that Sutardja and Nardi, individually or combined, do not teach each and every element as set forth in claim 10. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 10.

IV. Group IV: Claim 4

Claim 4 stands rejected as being obvious over Sutardja in view of Nardi. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section IV with respect to claim 4.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 4.

Claim 4 depends from claim 3. The arguments made in Section II with respect to claim 3 are made here in Section IV with respect to claim 4.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 4.

In addition, claim 4 recites "a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector". The Examiner has already admitted that "Sutardja fails to disclose a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector". Office Action Made Final of April 22, 2005 at page 4. The Board would expect, as would Appellants, that the Examiner would next explain how Nardi teaches a limiter as set forth in claim 4. Instead, the Examiner cut and paste the same summary of Nardi, regardless of claim language, that was also recited verbatim for claims 1, 3, 8, 10, 11, 15 and 17. Appellants respectfully draw the attention of the Board to the fact that the ubiquitous Nardi summary does not set forth a *prima facie* case of obviousness as to the limiter as set forth in claim 4. In fact, the word "limiter" is no where to be found in the oft-repeated Nardi summary.

Furthermore, as far back as the Response of June 1, 2004 at pages 3 and 4, Appellants have respectfully and specifically requested that the Examiner identify the limiter in Nardi. In the Reply After Final Rejection of June 22, 2005 at pages 2 and 3, in centered, bold lettering, Appellants again respectfully requested that the Examiner identify the limiter in Nardi. At no time during the prosecution of the present application has the Examiner ever once identified the limiter in Nardi. Appellants respectfully submit that the Examiner has failed in his burden to present a *prima facie* case of obviousness. Since the Examiner has not produce a *prima facie* case of obviousness, Appellants are under no obligation to submit further evidence of nonobviousness. See, e.g., M.P.E.P. § 2142.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 4.

V. Group V: Claim 11

Claim 11 stands rejected as being obvious over Sutardja in view of Nardi. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section V with respect to claim 11.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 11.

Claim 11 depends from claim 10. The arguments made in Section III with respect to claim 10 are made here in Section V with respect to claim 11.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 11.

In addition, claim 11 recites "a limiter coupled between the bandpass filter and the first input of the phase detector". The Examiner has already admitted that "Sutardja fails to disclose a limiter coupled between the bandpass filter and the first input of the phase detector". Office Action Made Final of April 22, 2005 at page 7. The Board would expect, as would Appellants, that the Examiner would next explain how Nardi teaches a

limiter as set forth in claim 11. Instead, the Examiner cut and paste the same summary of Nardi, regardless of claim language, that was also recited verbatim for claims 1, 3, 4, 8, 10, 15 and 17. Appellants respectfully draw the attention of the Board to the fact that the ubiquitous Nardi summary does not set forth a *prima facie* case of obviousness as to the limiter as set forth in claim 11. In fact, the word "limiter" is no where to be found in the oft-repeated Nardi summary.

Furthermore, as far back as the Response of June 1, 2004 at pages 3 and 4, Appellants have respectfully and specifically requested that the Examiner identify a limiter in Nardi. In the Reply After Final Rejection of June 22, 2005 at pages 2 and 3, in centered, bold lettering, Appellants again respectfully requested that the Examiner identify a limiter in Nardi. At no time during the prosecution of the present application has the Examiner ever once identified a limiter in Nardi. Appellants respectfully submit that the Examiner has failed in his burden to present a *prima facie* case of obviousness. Since the Examiner has not produce a *prima facie* case of obviousness, Appellants are under no obligation to submit further evidence of nonobviousness. See, e.g., M.P.E.P. § 2142.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 11.

VI. Group VI: Claim 18

Claim 18 stands rejected as being obvious over Sutardja in view of Nardi. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section VI with respect to claim 18.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 18.

In addition, claim 18 recites "means for limiting the filtered mixed signal from the filter means before being applied to the detector means". As already documented above with respect to claims 4 and 11, the oft-repeated Nardi summary does not present a *prima*

facie case of obviousness with respect to a limiter as set forth in claim 18. In fact, the word "limiter" is no where to be found in the oft-repeated Nardi summary.

As documented above, despite repeated requests that the Examiner identify a limiter in Nardi, it is a matter of record that, at no time during the prosecution of the present application, has the Examiner identified a limiter in Nardi. Appellants respectfully submit that the Examiner has failed in his burden to present a *prima facie* case of obviousness. Since the Examiner has not produce a *prima facie* case of obviousness, Appellants are under no obligation to submit further evidence of nonobviousness. See, e.g., M.P.E.P. § 2142.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 18.

VII. Group VII: Claim 7

Claim 7 stands rejected as being obvious over Sutardja in view of Nardi, and further in view of Hughes. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section VII with respect to claim 7.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on the combination of Sutardja and Nardi with respect to claim 7.

In addition, claim 7 recites "a bandpass filter to filter the mixed signal before being applied to the phase detector". Since at least these elements of claim 7 are the same as the elements recited above with respect to claim 3, the arguments made in Section II with respect to claim 3 are made here in Section VII with respect to claim 7. In addition, Hughes does not make up for the teaching deficiencies of Sutardja in view of Nardi. Hughes teaches that bandpass filter-amplifier means 74 is connected to receiver input 16a which is connected to the transmission medium, which in Hughes is power line 11. Thus, the incoming signal is immediately bandpass filtered before any mixing occurs. See, e.g., Hughes at FIG. 1A and 1C.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 7.

In addition, claim 7 recites "a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector". Since at least these elements of claim 7 are the same as the elements recited above with respect to claim 4, the arguments made in Section IV with respect to claim 4 are made here in Section VII with respect to claim 7. In addition, Hughes does not make up for the teaching deficiencies of Sutardja in view of Nardi. Hughes is silent as a limiter to limit a filtered mixed signal before being applied to a phase detector.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 7.

Furthermore, Appellants respectfully submit that Hughes teaches away from the alleged motivation for combining Sutardja, Nardi and Hughes which, according to the Examiner, "to employ a phase modulator in conjunction with a resonator in order to realize a phase locking oscillator circuit having a loop bandwidth broader than that of existing oscillator circuits". Office Action Made Final of April 22, 2005 at page 12. Nardi at FIG. 2 shows that the reason for expanding the loop bandwidth is because as phase noise of the reference oscillator 18 improves, to take advantage of the favorable phase noise plot as illustrated in FIG. 2, the loop bandwidth needs to be expanded beyond at least 10^6 radians. Compare this with Hughes, which is a power line communications system that operates at 60 Hz. To incorporate bandpass filter-amplifier means 74 of Hughes would effectively decrease loop bandwidth if the bandpass filter-amplifier means 74 were inserted into the Sutardja circuit modified by the Nardi circuit.

Appellants respectfully submit that one of ordinary skill in the art would not look to Hughes which operates at a system-wide frequency of 60 Hz for teachings to expand loop bandwidth beyond at least 10^6 radians. Furthermore, since the bandpass filter-amplifier means 74 is not part of phase lock loop 64 found in Hughes at FIG. 1D,

Appellants further challenge the motivation for taking bandpass filter-amplifier means 74 of Hughes and sticking it in a phase lock loop modified by Sutardja in view of Nardi as suggested by the Examiner.

Appellants further submit that Sutardja teaches power supply rejection capabilities to reduce phase noise and jitter as previously described above. Yet, Hughes teaches directly receiving signals from a power line which is an extremely noisy power supply. Respectfully, Hughes and Sutardja teach away from each other and should not be combined.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 7.

VIII. Group VIII: Claim 14

Claim 14 stands rejected as being obvious over Sutardja in view of Nardi, and further in view of Hughes. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section VIII with respect to claim 14.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on the combination of Sutardja and Nardi with respect to claim 14.

In addition, claim 14 recites "a limiter coupled between the bandpass filter and the first input of the phase detector". Since at least these elements of claim 14 are the same as the elements recited above with respect to claim 11, the arguments made in Section V with respect to claim 11 are made here in Section VIII with respect to claim 14. In addition, Hughes does not make up for the teaching deficiencies of Sutardja in view of Nardi. Hughes is silent as a limiter to limit a filtered mixed signal before being applied to a phase detector.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the

obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 14.

Furthermore, Appellants respectfully submit that Hughes teaches away from the alleged motivation for combining Sutardja, Nardi and Hughes which, according to the Examiner, "to employ a phase modulator in conjunction with a resonator in order to realize a phase locking oscillator circuit having a loop bandwidth broader than that of existing oscillator circuits". Office Action Made Final of April 22, 2005 at page 12. Nardi at FIG. 2 shows that the reason for expanding the loop bandwidth is because as phase noise of the reference oscillator 18 improves, to take advantage of the favorable phase noise plot as illustrated in FIG. 2, the loop bandwidth needs to be expanded beyond at least 10^6 radians. Compare this with Hughes, which is a power line communications system that operates at 60 Hz. To incorporate bandpass filter-amplifier means 74 of Hughes would effectively decrease loop bandwidth if the bandpass filter-amplifier means 74 were inserted into the Sutardja circuit modified by the Nardi circuit.

Appellants respectfully submit that one of ordinary skill in the art would not look to Hughes which operates at a system-wide frequency of 60 Hz for teachings to expand loop bandwidth beyond at least 10^6 radians. Furthermore, since the bandpass filter-amplifier means 74 is not part of phase lock loop 64 found in Hughes at FIG. 1D, Appellants further challenge the motivation for taking bandpass filter-amplifier means 74 of Hughes and sticking it in a phase lock loop modified by Sutardja in view of Nardi as suggested by the Examiner.

Appellants further submit that Sutardja teaches power supply rejection capabilities to reduce phase noise and jitter as previously described above. Yet, Hughes teaches directly receiving signals from a power line which is an extremely noisy power supply. Respectfully, Hughes and Sutardja teach away from each other and should not be combined.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 14.

IX. Group IX: Claim 21

Claim 21 stands rejected as being obvious over Sutardja in view of Nardi, and further in view of Hughes. The arguments made in Section I with respect to claims 1, 2, 5, 6, 8, 9, 12, 13, 15-17, 19 and 20 are also respectfully made here in Section IX with respect to claim 21.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on the combination of Sutardja and Nardi with respect to claim 21.

In addition, claim 21 recites "means for limiting the filtered mixed signal from the filter means before being applied to the detector means". Since at least these elements of claim 21 are the same as the elements recited above with respect to claim 18, the arguments made in Section VI with respect to claim 18 are made here in Section IX with respect to claim 21.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi with respect to claim 21.

Furthermore, Appellants respectfully submit that Hughes teaches away from the alleged motivation for combining Sutardja, Nardi and Hughes which, according to the Examiner, "to employ a phase modulator in conjunction with a resonator in order to realize a phase locking oscillator circuit having a loop bandwidth broader than that of existing oscillator circuits". Office Action Made Final of April 22, 2005 at page 12. Nardi at FIG. 2 shows that the reason for expanding the loop bandwidth is because as phase noise of the reference oscillator 18 improves, to take advantage of the favorable phase noise plot as illustrated in FIG. 2, the loop bandwidth needs to be expanded beyond at least 10^6 radians. Compare this with Hughes, which is a power line communications system that operates at 60 Hz. As alleged by the Examiner, to incorporate bandpass filter-amplifier means 74 of Hughes would effectively decrease loop bandwidth if the bandpass filter-amplifier means 74 were inserted into the Sutardja circuit modified by the Nardi circuit.

Appellants respectfully submit that one of ordinary skill in the art would not look to Hughes which operates at a system-wide frequency of 60 Hz for teachings to expand loop bandwidth beyond at least 10^6 radians. Furthermore, since the bandpass filter-amplifier means 74 (which the Examiner alleges is filter means with respect to claim 21) is not part of phase lock loop 64 found in Hughes at FIG. 1D, Appellants further challenge the motivation for taking bandpass filter-amplifier means 74 of Hughes and sticking it in a phase lock loop modified by Sutardja in view of Nardi as suggested by the Examiner.

Appellants further submit that Sutardja teaches power supply rejection capabilities to reduce phase noise and jitter as previously described above. Yet, Hughes teaches directly receiving signals from a power line which is an extremely noisy power supply. Respectfully, Hughes and Sutardja teach away from each other and should not be combined.

For at least the above reasons, it is respectfully submitted that an obviousness rejection cannot be maintained. It is respectfully requested that the Board reverse the obviousness rejection based on Sutardja in view of Nardi and further in view of Hughes with respect to claim 21.

X. Conclusion

For the foregoing reasons, claims 1-21 are patentable over the alleged prior art of record. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: October 25, 2005

Respectfully submitted,

Michael T. Cruz

Michael T. Cruz
Registration No. 44,636

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
Telephone: (312) 775-8084
Facsimile: (312) 775-8100

APPENDIX

The following claims are involved in this appeal:

1. A complimentary metal oxide semiconductor (CMOS) phase lock loop, comprising:

an oscillator having a tuning input, and an output with a tunable frequency responsive to the tuning input;

a mixer to mix the oscillator output with a second signal to produce a mixed signal; and

a phase detector outputting an error signal which is a function of a phase difference between the mixed signal and an input signal, the error signal being applied to the tuning input.

2. The CMOS phase lock loop of claim 1 wherein the oscillator comprises a voltage controlled oscillator, the tuning input being responsive to a voltage of the error signal.

3. The CMOS phase lock loop of claim 1 further comprising a bandpass filter to filter the mixed signal before being applied to the phase detector, the filtered mixed signal comprising a difference frequency between the tuned frequency of the oscillator output and a frequency of the second signal.

4. The CMOS phase lock loop of claim 3 further comprising a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector.

5. The CMOS phase lock loop of claim 1 further comprising a charge pump disposed between the phase detector and the oscillator.

6. The CMOS phase lock loop of claim 1 further comprising a loop filter disposed between the phase detector and the oscillator.

7. The CMOS phase lock loop of claim 1 wherein the oscillator comprises a voltage controlled oscillator, the tuning input being responsive to a voltage of the error signal, the CMOS phase lock loop further comprising a bandpass filter to filter the mixed signal before being applied to the phase detector, the filtered mixed signal comprising a difference frequency between the tuned frequency of the oscillator output and a frequency of the second signal, a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector, a charge pump disposed between the phase detector and the oscillator, and a loop filter disposed between the charge pump and the oscillator.

8. A complimentary metal oxide semiconductor (CMOS) phase lock loop, comprising:

a tunable oscillator having a tuning input;

a mixer coupled the oscillator; and

a phase detector having a first input coupled to the mixer, a second input adapted to receive an input signal, and an output coupled to the tuning input.

9. The CMOS phase lock loop of claim 8 wherein the oscillator comprises a voltage controlled oscillator.

10. The CMOS phase lock loop of claim 8 further comprising a bandpass filter coupled between the mixer and the first input of the phase detector.

11. The CMOS phase lock loop of claim 10 further comprising a limiter coupled between the bandpass filter and the first input of the phase detector.

12. The CMOS phase lock loop of claim 8 further comprising a charge pump coupled between the phase detector output and the tuning input of the oscillator.

13. The CMOS phase lock loop of claim 8 further comprising a loop filter coupled between the phase detector output and the tuning input of the oscillator.

14. The CMOS phase lock loop of claim 8 wherein the oscillator comprises a voltage controlled oscillator, the CMOS phase lock loop further comprising a bandpass filter coupled to the mixer, a limiter coupled between the bandpass filter and the first input of the phase detector, a charge pump coupled to the phase detector output, and a loop filter coupled between the charge pump and the tuning input of the oscillator.

15. A complimentary metal oxide semiconductor (CMOS) phase lock loop, comprising:

oscillator means for generating a first signal having a tunable frequency, the oscillating means comprising tuning means for tuning the frequency of the first signal;

mixer means for mixing the first signal with a second signal to produce a mixed signal; and

detector means for detecting a phase difference between the mixed signal and an input signal, and generating an error signal which is a function of the phase difference, the tuning means being responsive to the error signal.

16. The CMOS phase lock loop of claim 15 wherein the oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal.

17. The CMOS phase lock loop of claim 15 further comprising filter means for filtering the mixed signal before being applied to the detector means, the filtered mixed signal comprising a difference frequency between the tuned frequency of the first signal and a frequency of the second signal.

18. The CMOS phase lock loop of claim 17 further comprising means for limiting the filtered mixed signal from the filter means before being applied to the detector means.

19. The CMOS phase lock loop of claim 15 further comprising means for sourcing current to the tuning means responsive to the error signal.

20. The CMOS phase lock loop of claim 15 further comprising means for filtering the error signal from the detecting means before being applied to the tuning means.

21. The CMOS phase lock loop of claim 15 wherein the oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal, the CMOS phase lock loop further comprising filter means for filtering the mixed signal before being applied to the detector means, the filtered mixed signal comprising a difference frequency between the tuned frequency of the first signal and a frequency of the second signal, means for limiting the filtered mixed signal from the filter means before being applied to the detector means, current means for sourcing current to the tuning means responsive to the error signal, and means for filtering the current sourced error signal from the current means before being applied to the tuning means.